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EXAMINER	
IWASHKO, LEV	

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2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,204	TIAN, LIJUN	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-16 and 19-24* is/are rejected.

7)☐ Claim(s) *6,7,17,18 and 25-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 6-7, 17-18, and 25-27 are objected to as being dependent upon rejected base claims (1 and 4), (15), and (21 and 24) respectively, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010), further in view of Adelmann et al. (US Patent 4,703,477 A).

Lomp teaches the following limitations of claim 1:

Claim 1. A circuit, comprising:

- a hardware-based adaptive differential pulse code modulation (ADPCM) decoder; *(Column 55, lines 12-15 – State the following: "The SU further includes a Subscriber Line Interface 2310, including the functionality of a control (CC) generator, a Data Interface 2320, an ADPCM encoder 2321, an ADPCM decoder 2322")*

Adelmann teaches the rest of the limitations of claim 1 as follows:

- a memory storing both programming instructions and ADPCM encoded source file data; *(Column 24, lines 43-58 – State the following: "BDI to receive status translator 1904 includes a latch memory and read only memory unit (ROM) (not shown). The incoming BDI field is employed as an address to the ROM which provides the receive status (RS) signal and the packet length signal. Specifically, the receive status signal indicates*

the type of coding which was employed in the corresponding access interface transmitter. For example, whether it was 8-bit PCM coding, embedded ADPCM coding, that is, 413-bits embedded coding, 412-bits embedded coding, or 3/2-bits embedded coding, four-bit ADPCM, three-bit ADPCM or two-bit ADPCM. The length signal indicates the length of the packet to be played out of packet disassembler 1901, i.e., whether or not any of the enhancement bit fields have been dropped for the embedded coding packets")

- and a micro-controller having an architecture that implements time multiplexed memory addressing wherein ADPCM encoded source file data is extracted from the memory and delivered to the ADPCM decoder for processing in a first cycle, and wherein programming instructions are extracted from the memory and executed by the micro-controller in a second cycle while the hardware-based ADPCM decoder continues processing of the previously extracted ADPCM encoded source file data. *(Column 30, lines 45-68 and Column 31, lines 1-66 – State the following: "FIG. 25 shows in simplified block diagram form details of encoder 204 employed in voice processing module 201 of FIG. 2. Encoder 204 is employed to encode voiceband PCM signals, i.e., speech, voiceband data and tones into ADPCMsignals. In this example, 8-bit .mu.-law PCM signals are converted to linear form and, then, encoded into one of several possible ADPCM signals. For example, linear PCM samples may be converted into 4 bit, 3 bit or 2 bit ADPCM samples. Additionally, the ADPCM sames may include so-called embedded coding. For example, the output samples may be 4/2-bit embedded coding, 4/2-bit embedded coding or 3/2 bit embedded coding. As indicated above, such coding arrangements are knovn in the art. See, for example, U.S. Pat. No. 4,437,087 issued Mar. 13, 1984 for an adaptive ADPCM coding arrangement. Also, see U.S Pat. No. 4 519,073 issued May 21, 19B5 for a variable rate adaptive ADPCMcoding arrangement. Accordingly, in FIG. 25 linear PCM samples s.sub.1 (k) are supplied to a plus (+) input of difference circuit 2501 and a sample estimate s.sub.e (k) is supplied from adaptive predictor 2506 to a minus (-) input of difference circuit 2501 which generates a difference sample d(k). Difference sample d(k) is supplied to variable rate quantizer 2502 which, under control of a control signal supplied via bit rate controller form controller 207 (FIG. 2), generates the ADPCN output sample I(k). Variable rate quantizer 2502, in this example, includes three separate*

adaptive quantizers for generating either the 4-bit, 3-bit or 2-bit ADPCM sample I(k) under control of controller 207 (FIG. 2). Such adaptive quantizers are known in the art. See, for example, CCITT Recommendation G.721 "32 kbit/s Adaptive Differential Pulse Ccde Modulation (ADPCM)", VIIIth CCITT Plenary Assembly, Maloga-Torremolinos, Spain, Vol. 111, pp. 125-159, October 1984, for one such adaptive quantizer. The ADPCM sample I(k) is supplied to quantizer adaptation unit 2503, variable rate inverse quantizer 2504 and to packet assembler 202 (FIG. 2). Variable rate inverse quantizer 2504 also includes three adaptive inverse quantizers which perform the inverse functions of the adaptive quantizers of variable rate quantizer 2502 and generate a quantized version of the difference sample, namely, d.sub.q (k). Again, the particular one of the inverse quantizers that is used is under control of control signals supplied via bit rate controller 2510 from controller 207 (FIG. 2). The adaptive inverse quantizers are, in this example, 4-bit, 3-bit and 2-bit and are selected depending on the particular coding being used. For example, if 4/2-bit embedded coding is being used in a particular time slot, a 4-bit adaptive quantizer is selected in variable rate quantizer 2502 and a 2-bit variable rate adaptive inverse quantizer is selected in variable rate inverse quantizer 2504. An example of an adaptive inverse quantizer that may be employed in variable rate inverse quantizer 2504 is disclosed in the CCITT Recommendation G.721 cited above. The quantized version of the difference sample d.sub.q (k) is supplied to one input of summing circuit 2505 and the sample estimate is supplied to another input of summing circuit 2505 which provides the algebraic sum thereof at its output, namely, reconstructed sample s.sub.r (k). The reconstructed sample s.sub.r (k) is supplied to adaptive predictor 2506. Adaptive predictor 2506 generates estimate sample s.sub.e (k) which is an estimate of the linear PCM input sample s.sub.l (k). One such adaptive predictor is also disclosed in the CCITT Recommendation C.721 cited above. Variable rate quantizer adaptation unit 2503 generates the quantizer and inverse quantizer adaptation scale factors y.sub.a (k) and Y.sub.b (k), respectively. Scale factor y.sub.a (k) is supplied to the variable rate quantizer 2502 and scale factor y.sub.b (k) is supplied to variable rate inverse quantizer 2504. Again, variable rate quantizer adaptation unit 2503 includes three quantizer adaptation units, in this example, one for 4-bit, one for 3-bit and one for 2-bit quantization. The selection of the particular

one or ones of the quantizer adaptation units is also under control of control signals supplied via bit rate controller 2510 from controller 207 (FIG. 2). By way of an example, if 4/2-bit embedded coding is being used, 4bit scale factor y.sub.a (k) adaptation is selected for variable rate quantizer 2502, and 2-bit scale factor y.sub.b (k) adaptation is selected for variable rate inverse quantizer 2504. As is apparent, the scale factor adaptation selected under control of controller 207 has to match the adaptive quantizer selected in variable rate quantizer 2502 and also the inverse adaptive quantizer selected in variable rate inverse quantizer 2504. One such quantizer adaptation unit including an adaptation speed control and a quantizer scale factor adaptation unit is disclosed in the CCITT Recommendation G.721 cited above")

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Code Division Multiple Access System" of Lomp and the "Packet Information Field Data Format" of Adelmann before him at the time the invention was made, combine the inventions so that the system would be more efficient and accurate.

4. Claim 2 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010) and Adelmann et al. (US Patent 4,703,477 A), as applies to Claim 1 above.

Lomp teaches the limitations of Claim 2 as follows:

Claim 2. The circuit of claim 1 wherein the hardware-based ADPCM decoder operates to synthesize decoded output data from the extracted ADPCM encoded source file data without any processing assistance from the micro-controller. *(Column 55, lines 44-47 and 50-54 – State the following: "If the coding signal indicates the traffic message is ADPCM coded, the traffic message RVMESS is sent to the ADPCM decoder 2322 by sending a select message to the Data Interface 2320." "The traffic message signal RVMESS is the input signal to the ADPCM decoder 2322, where the traffic message signal is converted to a digital information signal RINF in response to the values of the input ADPCM coding signal")*

5. Claim 3 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010) and Adelmann et al. (US Patent 4,703,477 A), as applies to Claim 1 above.

Adelmann teaches the limitations of Claim 2 as follows:

> Claim 3. The circuit of claim 2 wherein the decoded output data comprises linear pulse code modulation (PCM) format data. *(Column 34, lines 1-3 – State the following: "In this example, 4-bit, 3-bit or 2-bit ADPCM samples are decoded into linear PCM form")*

6. Claim 4 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010) and Adelmann et al. (US Patent 4,703,477 A) as applies to claim 1, further in view of Childers et al. (US Patent 5,105,387 A) and Zeilenga et al. (US Patent 5,144,242 A).

Lomp and Adelmann teach the limitations of claim 1 as stated above.

Childers teaches a portion of claim 4 as follows:

> Claim 4. The circuit of claim 1 wherein the architecture of the micro-controller comprises:
> - a program counter that supplies a memory address for retrieving micro-controller programming instructions; *(Column 45, lines 55-67 and Column 46, lines 1-6 – State the following: "In FIG. 53, a SVP controller having ROM memory, for example, is depicted on association with circuitry fore reducing memory requirements of the controller memory. Briefly, this reduction is achieved by adding repeat counter 1588 and count/hold input to program counter 1584 to controller as depicted. The controller data and address locations are sequenced by the N-bit output of the program counter. The program counter is clocked and reset via signal inputs 1596 and 1598 respectively. The controller provides a plurality of output signals: 4-bit count signal 1600 which is input to repeat counter 1588 allow a repeat count up to 16; the 24-bit opcode 1602 also referred to as microcode or microinstructions which are latched via latch 1590; 7b-t address 1604, which is used by the up counter 1592 for the RF0 operand address; a similarly 7-bit address 1606, which is used by the provided via RF1 address up counter 1594. Additionally, a 1-bit control signal 1607 is provided to control logic 1586 to indicate whether a single or double instruction is being implemented")*
> - an address counter that supplies a memory address for retrieving a portion of the ADPCM encoded source file data; *(Column 41, lines 40-44 – State the following: : "Global*

rotation address generator 1246 receives a relative register address from the register file 0 address counter via lines 1291. This relative address is provided to address register locations in register file 0 via lines 948")

Zeilenga teaches a portion of claim 4 as follows:

- and a multiplexer connected to the program counter and the address counter and operating to select between program counter and address counter supplied memory addresses. *(Column 26, lines 1-4 – State the following: "Meanwhile, the signal /RAMADD is asserted to control memory address multiplexer 1100 to select a ROW address provided by row counter 900 instead of the PC output of program counter 500")*

7. Claim 5 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010), Adelmann et al. (US Patent 4,703,477 A), Childers et al. (US Patent 5,105,387 A), and Zeilenga et al. (US Patent 5,144,242 A) as applies to claims 1 and 4, further in view of Lesmeister et al. (US Patent 5,931,952).

Lomp, Adelmann, Childers, and Zeilenga teach the limitations of claims 1 and 4.

Lomp, Adelmann, Childers, and Zeilenga's inventions differ from the claimed invention as the make no reference to signal phases.

Lomp, Adelmann, Childers, and Zeilenga fail to teach claim 5, which states "The circuit of claim 4 wherein the selection operation of the multiplexer is driven by a two phase clock signal having a first phase for selecting the address counter and a second phase for selecting the program counter." However, Lesmeister states "The apparatus in accordance with claim 1 wherein said control signal assertion means comprises: multiplexer means receiving said timing signals for producing an output timing signal in phase with one of said timing signals selected in accordance with each said command" (Column 28, lines 23-27). It would have been obvious to one skilled in the art at the time of the applicant's invention, to combine the "Code Division

Multiple Access System" of Lomp, the "Packet Information Field Data Format" of Adelmann, the "Three Transistor Dual Access Port Dynamic Random Access Memory Gain Cell" of Childers, the "Continually Loadable Microcode Store for MRI Control Sequencers" of Zeilenga, and Lesmeister's "Parallel Processing Integrated Circuit Tester" so that the system would have a mux with two phases that would select between aforementioned counters, thereby enhancing system efficiency.

8. Claim 8 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010) as applies to claim 1, further in view of Adelmann et al. (US Patent 4,703,477 A).

Adelmann teaches claim 8 as follows:

> Claim 8. The circuit of claim 1 wherein the first and second cycles consecutively repeat until all ADPCM encoded source file data is extracted for decoder processing. *(Column 7, lines 35-47 – State the following: "The ADPCM output from encoder 204 is supplied to formatter 209 in packet assembler 202. Formatter 209 includes, in this example, a RAM memory unit and a plurality of counters (not shown) which perform a shift register function for the purpose of rearranging the supplied bits into a packet information field format as shown in FIGS. 3 and 4 for the .mu.-law PCM signal format and for the 32 kilobit/sec ADPCM signal format, respectively. It should be noted that FIGS. 3 and 4 depict the formats for an individual time slot, for example, time slot zero, and are repeated for the remaining time slots 1 through 31 in each frame of the PCM transmit signals")*

It would have been obvious to one skilled in the art at the time of the applicant's invention, to combine the "Code Division Multiple Access System" of Lomp and the "Packet Information Field Data Format" of Adelmann to include repetition until completion for the cycles, so that there would be an actual termination of events, thereby eliminating a potential infinite loop.

9. Claim 9 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010) and Adelmann et al. (US Patent 4,703,477 A), as applies to Claim 1 above.

Adelmann teaches the limitations of Claim 9 as follows:

> Claim 9. The circuit of claim 1 wherein the memory comprises a read only memory (ROM). *(Column 24, lines 43-58 – State the following: "BDI to receive status translator 1904 includes a latch memory and read only memory unit (ROM) (not shown). The incoming BDI field is employed as an address to the ROM which provides the receive status (RS) signal and the packet length signal. Specifically, the receive status signal indicates the type of coding which was employed in the corresponding access interface transmitter. For example, whether it was 8-bit PCM coding, embedded ADPCM coding, that is, 413-bits embedded coding, 412-bits embedded coding, or 3/2-bits embedded coding, four-bit ADPCM, three-bit ADPCM or two-bit ADPCM. The length signal indicates the length of the packet to be played out of packet disassembler 1901, i.e., whether or not any of the enhancement bit fields have been dropped for the embedded coding packets")*

10. Claim 10 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010) and Adelmann et al. (US Patent 4,703,477 A), as applies to Claim 1 above.

Lomp and Adelmann teach Claim 1 as stated above.

Lomp and Adelmann's inventions differ from the proposed invention as they do not state that the system can be placed on a single integrated chip.

Lomp and Adelmann fail to teach Claim 10, which states "The circuit of claim 1 wherein the circuit is fully implemented on an integrated circuit chip." However, in this case, making parts of a whole integral (as would be done on this chip), does not change the purpose or functionality of the invention as far as the claims are concerned. Therefore, it would have been obvious to include the "Code Division Multiple Access System" of Lomp and the "Packet

Information Field Data Format" of Adelmann on one circuit board to preserve space on a motherboard.

For further information please reference, In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) (A claim to a fluid transporting vehicle was rejected as obvious over a prior art reference which differed from the prior art in claiming a brake drum integral with a clamping means, whereas the brake disc and clamp of the prior art comprise several parts rigidly secured together as a single unit. The court affirmed the rejection holding, among other reasons, "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice."); but see Schenck v. Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983) (Claims were directed to a vibratory testing machine (a hard-bearing wheel balancer) comprising a holding structure, a base structure, and a supporting means which form "a single integral and gaplessly continuous piece." Nortron argued that the invention is just making integral what had been made in four bolted pieces. The court found this argument unpersuasive and held that the claims were patentable because the prior art perceived a need for mechanisms to dampen resonance, whereas the inventor eliminated the need for dampening via the one-piece gapless support structure, showing insight that was contrary to the understandings and expectations of the art.).

11. Claims 11-14 are rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010), Adelmann et al. (US Patent 4,703,477 A), Childers et al. (US Patent 5,105,387 A), and Zeilenga et al. (US Patent 5,144,242 A), further in view of Lesmeister et al. (US Patent 5,931,952).

Since the material in Claims 11-14 directly correlates to a method of producing what is claimed in Claims 1-5, the same rejections from the aforementioned Claims 1-5 apply.

12. Claim 15 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010) and Adelmann et al. (US Patent 4,703,477 A), further in view of Childers et al. (US Patent 5,105,387 A) and Zeilenga et al. (US Patent 5,144,242 A).

Lomp and Adelmann teach a portion of claim 15 as follows:

> Claim 15. A programming architecture for a micro-controller connected to a memory storing both programming instructions and adaptive differential pulse code modulation (ADPCM) encoded source file data, the architecture comprising: *(Column 55, lines 12-15 – State the following: "The SU further includes a Subscriber Line Interface 2310, including the functionality of a control (CC) generator, a Data Interface 2320, an ADPCM encoder 2321, an ADPCM decoder 2322")*

Childers teaches a portion of claim 14 as follows:

- a program counter storing a first memory address relating to a micro-controller programming instruction; *(Column 45, lines 55-67 and Column 46, lines 1-6 – State the following: "In FIG. 53, a SVP controller having ROM memory, for example, is depicted on association with circuitry fore reducing memory requirements of the controller memory. Briefly, this reduction is achieved by adding repeat counter 1588 and count/hold input to program counter 1584 to controller as depicted. The controller data and address locations are sequenced by the N-bit output of the program counter. The program counter is clocked and reset via signal inputs 1596 and 1598 respectively. The controller provides a plurality of output signals: 4-bit count signal 1600 which is input to repeat counter 1588 allow a repeat count up to 16; the 24-bit opcode 1602 also referred to as microcode or microinstructions which are latched via latch 1590; 7b-t address 1604, which is used by the up counter 1592 for the RF0 operand address; a similarly 7-bit address 1606, which is used by the provided via RF1 address up counter 1594. Additionally, a 1-bit control signal 1607 is provided to control logic 1586 to indicate whether a single or double instruction is being implemented")*

- an address counter storing a second memory address relating to a portion of the ADPCM encoded source file data; *(Column 41, lines 40-44 – State the following: : "Global rotation address generator 1246 receives a relative register address from the register file 0 address counter via lines 1291. This relative address is provided to address register locations in register file 0 via lines 948")*

Zeilenga teaches the rest of the limitations of claim 15 as follows:

- a multiplexer receiving the first and second memory addresses and operating to select the first memory address for application to the memory during a first cycle and operate to select the second memory address for application to the memory during a second cycle. *(Column 26, lines 1-4 – State the following: "Meanwhile, the signal /RAMADD is asserted to control memory address multiplexer 1100 to select a ROW address provided by row counter 900 instead of the PC output of program counter 500")*

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Code Division Multiple Access System" of Lomp and the "Packet Information Field Data Format" of Adelmann, "Three Transistor Dual Access Port Dynamic Random Access Memory Gain Cell" of Childers, and the "Continually Loadable Microcode Store for MRI Control Sequencers" of Zeilenga before him at the time the invention was made, combine the inventions so that the system would be more efficient and accurate.

13. Claim 16 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010), Adelmann et al. (US Patent 4,703,477 A), Childers et al. (US Patent 5,105,387 A), and Zeilenga et al. (US Patent 5,144,242 A) as applies to claim 15, further in view of Lesmeister et al. (US Patent 5,931,952).

Lomp, Adelmann, Childers, and Zeilenga teach the limitations of claim 15.

Lomp, Adelmann, Childers, and Zeilenga's inventions differ from the claimed invention as the make no reference to signal phases.

Lomp, Adelmann, Childers, and Zeilenga fail to teach claim 16, which states "The programming architecture of claim 15 further comprising a clock signal having a first and second phase to drive operation of the multiplexer selection between the first and second memory addresses, respectively." However, Lesmeister states "The apparatus in accordance with claim 1 wherein said control signal assertion means comprises: multiplexer means receiving said timing signals for producing an output timing signal in phase with one of said timing signals selected in accordance with each said command" (Column 28, lines 23-27). It would have been obvious to one skilled in the art at the time of the applicant's invention, to combine the "Code Division Multiple Access System" of Lomp, the "Packet Information Field Data Format" of Adelmann, the "Three Transistor Dual Access Port Dynamic Random Access Memory Gain Cell" of Childers, the "Continually Loadable Microcode Store for MRI Control Sequencers" of Zeilenga, and Lesmeister's "Parallel Processing Integrated Circuit Tester" so that the system would have a mux with two phases that would select between aforementioned counters, thereby enhancing system efficiency.

14. Claim 19 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010), Adelmann et al. (US Patent 4,703,477 A), Childers et al. (US Patent 5,105,387 A), and Zeilenga et al. (US Patent 5,144,242 A) as applies to claim 15.

Childers teaches the following limitations of claim 19:

> Claim 19. The programming architecture of claim 15 further including a first increment signal applied to the address counter to increment the second memory address during the second cycle to consecutively access all portions of the ADPCM encoded source file data.

(Column 46, lines 48-51 – State the following: "When the repeat counter is engaged, the program counter stops and the two address counters auto-increment 1 for signals instructions or by 2 for double instructions")

15. Claim 20 is rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010), Adelmann et al. (US Patent 4,703,477 A), Childers et al. (US Patent 5,105,387 A), and Zeilenga et al. (US Patent 5,144,242 A) as applies to claims 15 and 19.

Zeilenga teaches the following limitations of claim 20:

Claim 20. The programming architecture of claim 19 further including a second increment signal applied to the program counter to increment the first memory address during the first cycle to change the micro-controller programming instruction. *(Column 15, lines 41-54 – State the following: "Sequencer control section (SCS) 400 in the preferred embodiment provides synchronization and control signals for the remainder of sequencer 140. There is a very close degree of interaction between SCS 400 and each of the other blocks of sequencer 140 such that individual control signals (not shown in FIG. 6) flow directly between each of the other functional blocks and the SCS. In addition, the preferred embodiment sequencer architecture includes internal busses BCON and BBUF providing control signal paths between the SCS 400 and the various other functional blocks of the sequencer 140. One of the blocks intimately coupled to SCS 400 is a 15-bit auto-increment program (location) counter")*

16. Claims 21-24 are rejected under 35 U.S.C.103(a) as being unpatentable over Lomp et al. (US Patent 5,799,010), Adelmann et al. (US Patent 4,703,477 A), Childers et al. (US Patent 5,105,387 A), and Zeilenga et al. (US Patent 5,144,242 A), further in view of Lesmeister et al. (US Patent 5,931,952).

Since the material in Claims 21-24 directly correlates to the system of Claim 1 appearing on a single integrated circuit chip, the same rejections from the aforementioned Claims 1-4 apply. Furthermore, the rejection of Claim 10 also applies here, as these claims include the

system on a single integrated circuit chip, which does not change the purpose or functionality of the invention.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER